Physical Design Implementation LDO

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Abstract **- This project aims to implement a LDO on physical design flow from netlist to GDSII that starts from floorplan, placement, CTS, routing and ends with physical verification checks such as DRC, LVS and ERC, antenna design rule. Floorplanning is the basic building step for any hierarchical physical design flow. Floorplanning is taking more amount of time in entire design hierarchical flow. If floorplanning is not good the entire design will take more time and it will increase a greater number of iterations to complete the design. In this paper we have demonstrated different physical design techniques to optimize the area and fit the same design on optimized die size without compromising on the design features. With these physical design techniques one can optimize the design and reduce the area and thereby increase the chip margin from silicon point of view.**

Index Terms **- LDO, Physical Design, VLSI, Synopsys, ICC.**

1.INTRODUCTION

As per the Moores law we see that the todays ICs are getting more and more feature on the same unit area. Along with this the demand to add as much possible as design features is increasing. This requires an increase in silicon area. But the cost of the silicon is directly proportional to the area of the silicon. Hence area of silicon plays an important role for any SoC both from features point of view and cost point of view. So we need to have good floorplan for reducing the area with excellent performance. In this project we had a good floorplan of standard cell library. And we have taken the netlist from open source.

Floorplanning is the most important step in the PD flow. The quality of the Floorplanning is effect on further stages of placement, cts, routing. If the Floorplanning is not in good manner then further stages are facing various problems like less availability of routing resources, it is difficult to meet the desire timing requirements which results in more number of iterations and takes more memory for the design and CPU runtime.

2. INTRODUCTION TO PHYSICAL DESIGN

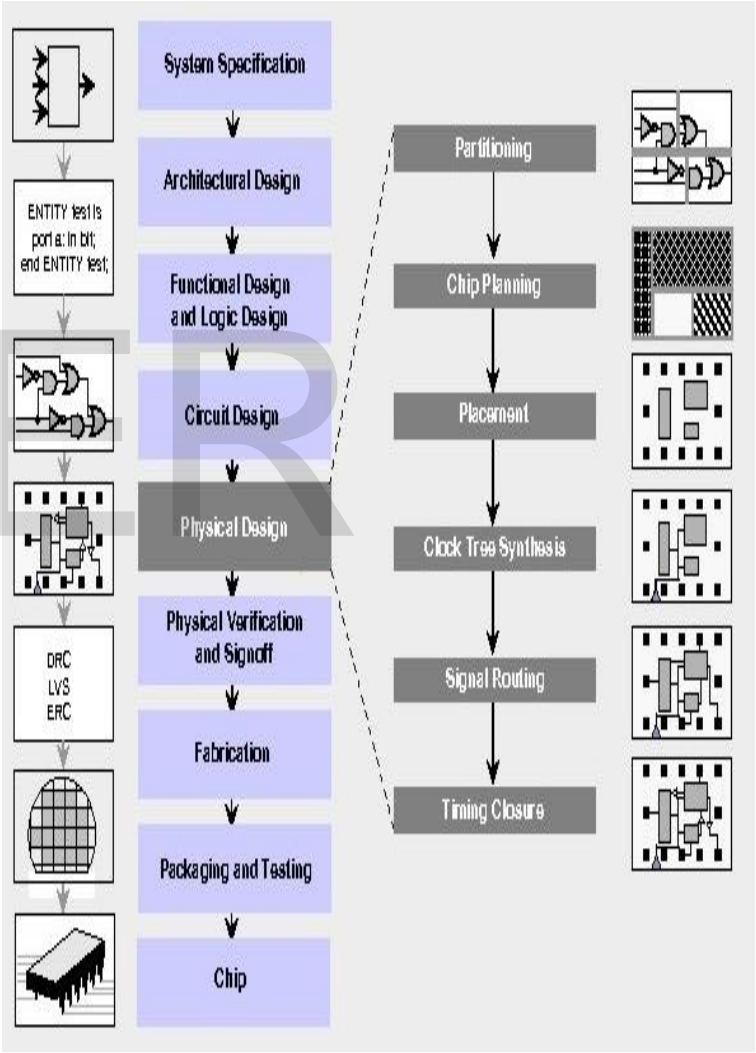


Fig 1 : Flow of Physical Design

2.1 INPUTS TO PHYSICAL DESIGN

1.Logical libraries →format is .lib→ given by vendor

2.Physical Libraries →format is .lef → given by vendor

3.Tech file →format is .tf → given by fabrication people

4.TLU+file →format is .TLUP→ given by fabrication people

5.Netlist →format is .v → given by synthesis people

6.Synthesis Design Constraints→format is .sdc → given by synthesis people

2.2FLOORPLAN

Floorplanning is the art of any physical design. A well and perfect floorplan leads to an ASIC design with higher performance and optimum area. Floorplanning can be challenging in that, it deals with the placement of I/O pads and macros as well as power and ground structure. Before we are going for the floor planning to make sure that inputs are used for floorplan is prepared properly.

2.3 PLACEMENT

Placement is the process of finding a suitable physical location for each cell in the block. Tool only determine the location of each standard cell on the die. Placement does not just place the standard cell available in the synthesized netlist, it also optimized the design

2.4 CLOCK TREE SYNTHESIS (CTS)

CTS is the process of connecting the clocks to all clock pin of sequential circuits by using inverters/buffers in order to balance the skew and to minimize the insertion delay. All the clock pins are driven by a single clock source. Clock balancing is important for meeting all the design constraints.

2.5 ROUTING

After the floorplanning and placement steps in the design, routing needs to be done. Routing is nothing but connecting the various blocks in the chip with one another. Until now, the blocks were only just placed on the chip. Routing also is spilt into two steps

3. LOW DROP OUT REGULATOR

A **low-dropout regulator** (**LDO regulator**) is a DC linear voltage regulator that can regulate the output voltage even when the supply voltage is very close to the output voltage.

The advantages of a low dropout voltage regulator over other DC to DC regulators include the absence of switching noise (as no switching takes place), smaller device size (as neither large inductors nor transformers are needed), and greater design simplicity (usually consists of a reference, an amplifier, and a pass element). The disadvantage is that, unlike switching regulators, linear DC regulators must dissipate power, and thus heat, across the regulation device in order to regulate the output voltage.

The main components are a power FET and a differential amplifier (error amplifier). One input of the differential amplifier monitors the fraction of the output determined by the resistor ratio of R1 and R2. The second input to the differential amplifier is from a stable voltage reference (bandgap reference). If the output voltage rises too high relative to the reference voltage, the drive to the power FET changes to maintain a constant output voltage

We can see below, The complete design of the LDO chip becomes

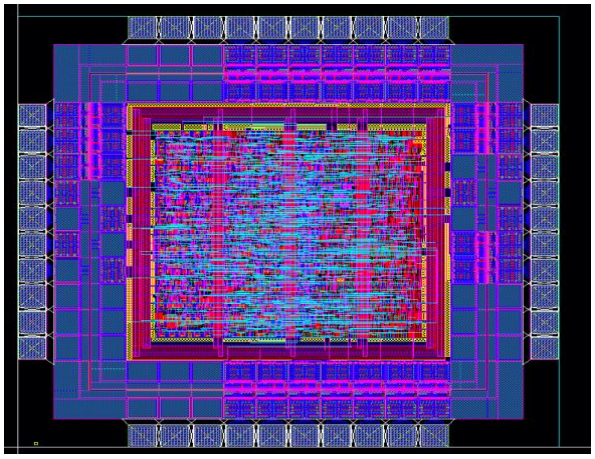


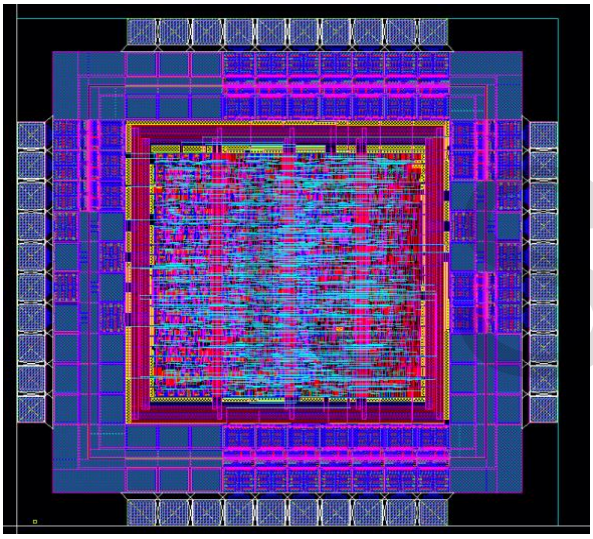
Fig 2 : Physical Design Implementation of LDO

4. RESULT

4.1 GDSII

The Physical design of the output is GDSII file. After completion of Physical verification we have to save our design in GDSII format. So below is the view of the our project design after this our gdsii file will go to the fab.

Before sending to fabrication, the chip needs to be verified with the schematic and with the DRC rules (DRC and LVS), other post-layout analysis will not be made in this post. The pads rules are not the same as the standard rules for the technology, for this reason, it is required to remove the pads in order to successfully run the DRC and LVS to check if the core is functional. To do so, create a clone of the hole library, and remove the pads from the layout and schematic of the clone



The above layout were sent to fabrication (MOSIS) after adjusting the DRC errors such as tiling, and the LVS too. I will make a post with the testing of the physical chip soon.

5.CONCLUSION

The physical design flow of a LDO from netlist to gdsii that starts from floorplan, placement, CTS, routing and ends with physical verification was implemented. The violations those resulted in the implementation of LDO such as crosstalk, slew violations, congestion and other signal integrity issues are fixed by inserting additional buffers as well as using double width double spacing rule. For this implementation Synopsys ICC tool is used. Results show that the implemented design clears the physical verification checks such as DRC, LVC and antenna design rule to obtain a design that is suitable for manufacturing.

6.REFERENCES

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